Buffered SC/MP - MP.A.7

Function.

This board provides a fully buffered SC/MP processor with a full 16 bit address bus. Additional components may be added to allow slow memory to be used and to provide single cycle/instruction modes.

Operation.

The SC/MP data bus is buffered using IC1 & 6 and the read and write strobes (NRDS & NWDS) which enable the appropriate buffer for the direction of data transfer required. The low order address lines are buffered by IC2 & 3, whereas the high order address signals are first latched from the data bus by IC8 and then buffered by IC4. The read and write strobes are also buffered by IC4. The system clock is derived using half of IC9 and a quartz crystal.

Slow memory may be accommodated by adding wait states using a shift register IC15. The register is loaded at NADS time with a bit pattern defined using the switches W1-4. The data is then shifted out serially using the system clock. If a low is shifted out to the NHOLD line before the end of the read/write strobe then the strobe is extended until NHOLD returns high. Normally the strobes are three clock periods long so the first three bits loaded into the shift register are also set low. When W1 -4 are open no wait states are added, but as the switches are closed one by one extra wait states are to the strobe pulses.

The HALT flag is decoded using IC12 and causes the processor to stop by resetting a flip-flop (half of IC11) and setting the CONT input of the processor low. The processor may be restarted by depressing the GO switch. IC13 is used to debouce this switch and this then clocks a high level onto the outputs of IC11 and allows processor operation to continue.

The single cycle/instruction logic works by allowing NADS to clear either flip-flop of IC11. In the single instruction mode the CONT line is pulled low by the first NADS pulse. This causes operation to be halted after the current instruction has been completed. In the single cycle mode NHOLD is pulled low by each NADS pulse so that a prolonged wait state is entered with every processor data transfer. In the single cycle/ instruction mode displays should be connected to the data buses via suitable buffers (especially 4050) so that the the address and data on the buses can be read directly. Sucessive cycles/instructions are executed by pressing the GO switch. The RDY (ReaDY) switch may be used to initialise the logic at the start of single cycle operation. On power up it it generally necessary to press GO as the flip-flops of IC11 tend to power up with their outputs set low.

Options.

1. Buffered processor only.

Fit IC's 1-10, R1-7, C1-5 only.

2. Adding wait states.

Add IC15, R8-11, C7-8. A dual in line switch or wire links may be used for W1-4. Insert L1 and cut the small track connecting one of the L1 pads to a wider track running from IC11 to IC10 between L1 pads.

3. Single cycle mode.

Add IC11-14, R12-17, C6. Omit L1 unless wait states are also being added (see 2. above).

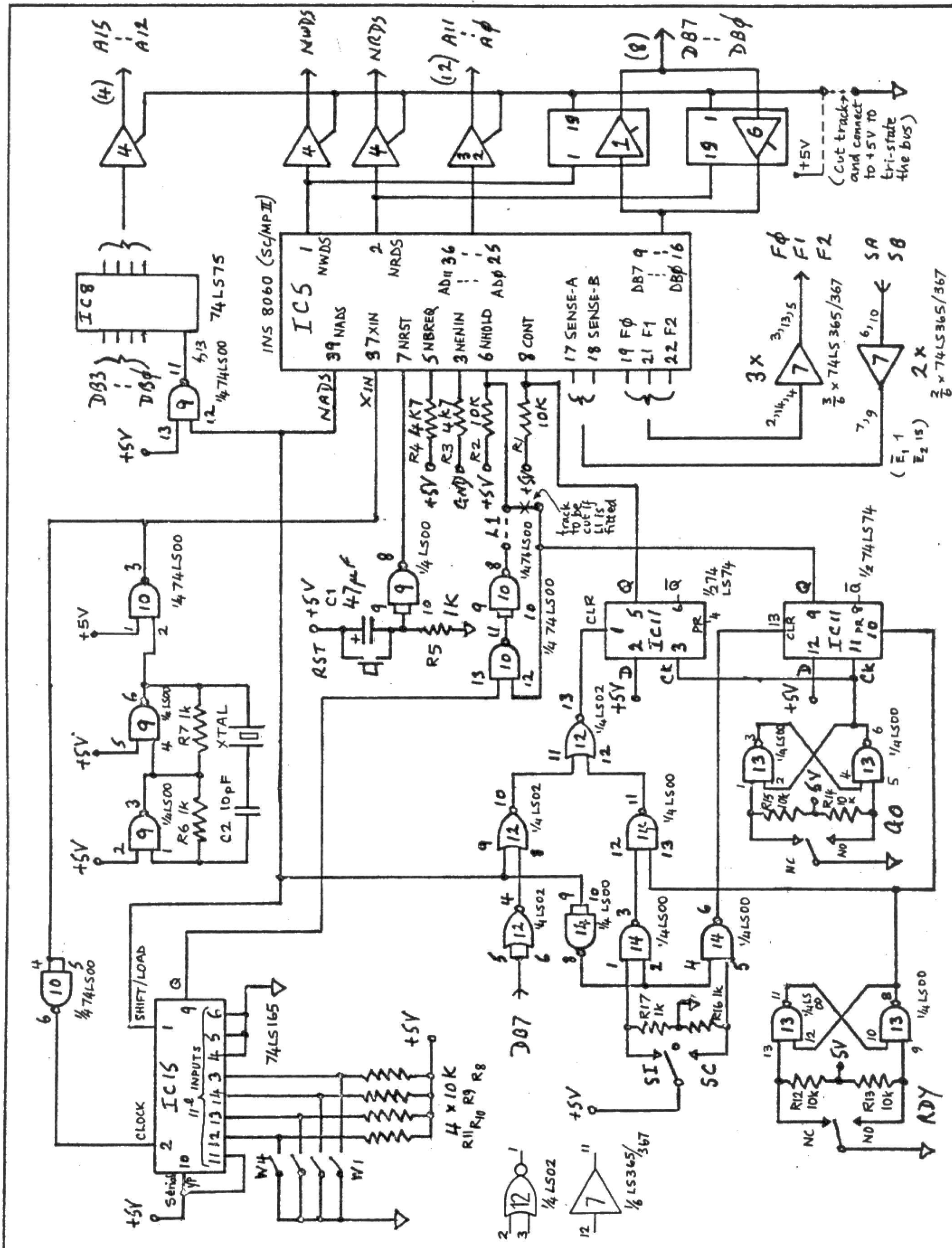
4. Tristating the bus.

All the bus signals may be tristated by connecting the control point G to +5V and cutting the track between point G and the through hole link connecting IC8 pin 20 to Ground. This is useful in multiprocessor applications.

5. Halt indicator.

A halt state indicator may be usefully added by taking the signal from pin 6 of IC11 and using this to drive an LED via a suitable transistor.

JSD 10.7.79



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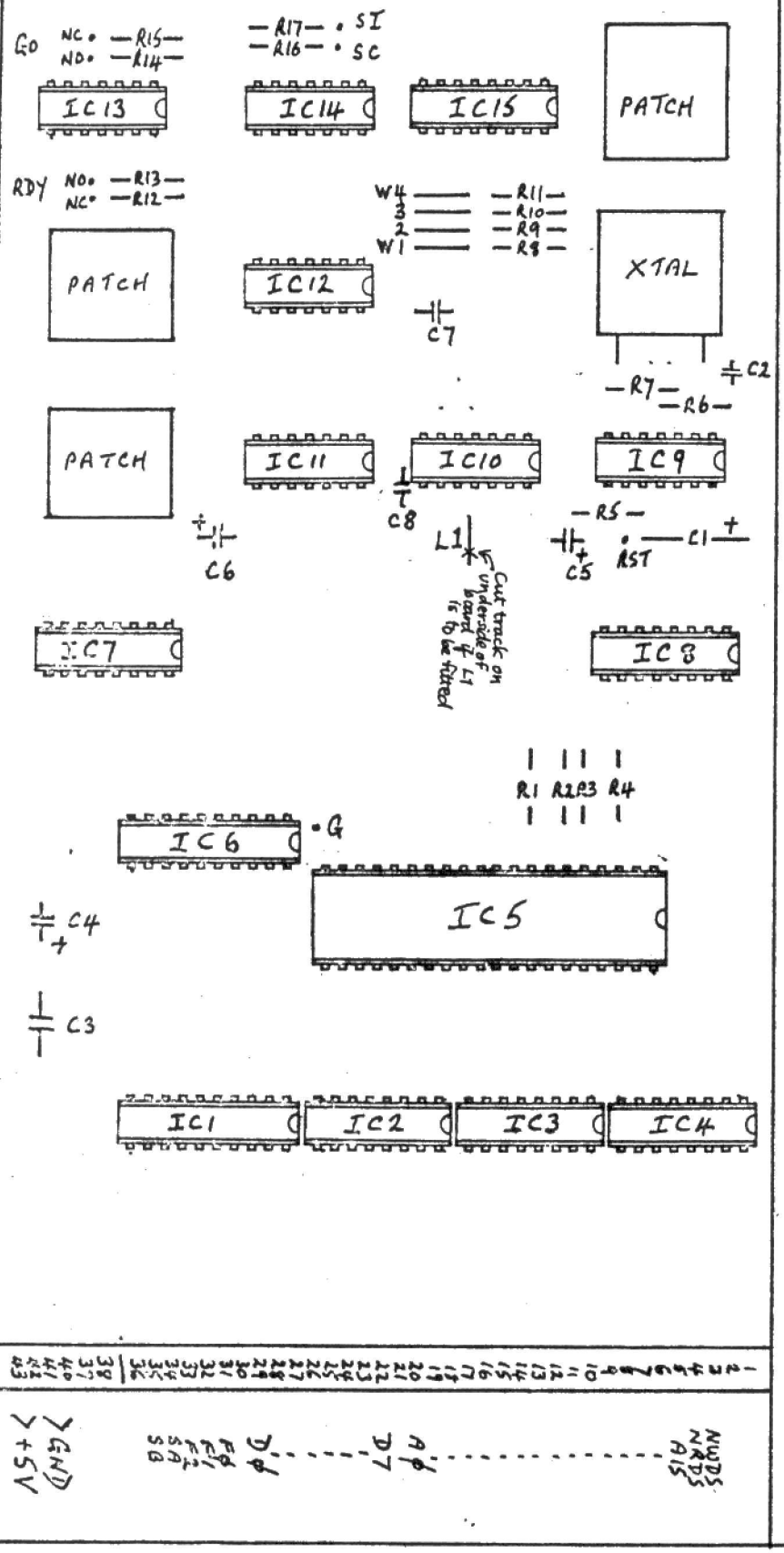

COMPONENTS

R1	10K	R10	10K
2	10K	11	10K
3	4K7	12	10K
4	4K7	13	10K
5	1K	14	10K
6	1k	15	10K
7	1k	16	1K
8	10K	17	1K
9	10K		

C1	47μ, 10V	C6	10μF
2	10pF	C7	0·1μ Disc
3	0·1μ Disc	C8	0·1μ "
4	100μF		ELECTROLYTICS 10V
5	10μ		

IC1	81LS95	IC8	74LS75
2	74LS365	9	74LS00
3	74LS365	10	74LS00
4	74LS365	11	74LS74
5	INS 8060	12	74LS02
6	81LS95	13	74LS00
7	74LS365/367	14	74LS00
		15	74LS165

SWITCHES :-

GO - S.P.D.T - WIPER GND

RDY - S.P.D.T - WIPER GND

SI/SC - CENTRE OFF - WIPER +5V S.P.D.T.

W1 - W4 MAY BE DIL SWITCH (CONTROL WAIT STATES)

RST SWITCH - MOMENTARY ACTION TO +5V.

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